ABSTRACT OF THE DISCLOSURE

Clock control of a sequential circuit is realized with the assumptions that stop of a clock is impossible due to the specifications, and feedback of the output of a memory element does not exist. To this end, the sequential circuit includes a variation detector for detecting a variation occurred in the content of any of master cells which are memory elements included in a master cell group to output a clock control signal, and a clock pulse generator for receiving the clock control signal to generate a clock pulse and supplying the clock pulse to a slave cell which is a memory element included in a clock domain and whose input is varied when the content of any of the master cells which are memory elements included in the master cell group is varied.